

### General Description

The CXL-SD1D150S is a large single digit seven segment display module that uses Ntera Nano-chromics technology. This enables a reflective display to be produced which has vivid blue segments on a white background. The display has a superb contrast ratio, exceptionally wide viewing angle and ink on paper style visibility.

With a minimum input voltage of 3.7V and a quiescent current of 45uA it is ideally suited for battery powered operation.

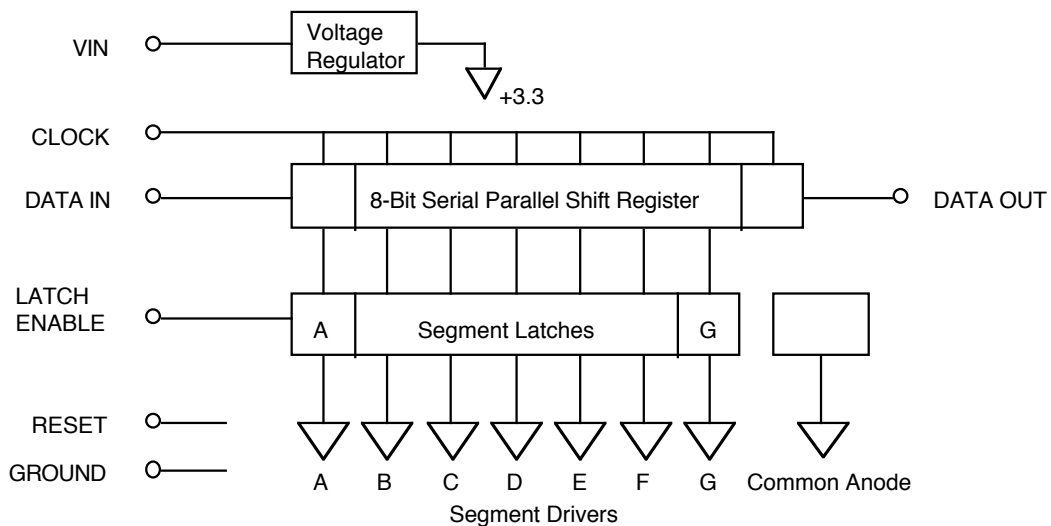
Simple to drive from a standard micro-controller SPI interface or using 3 GPIO pins, it can be cascaded for multi-digit displays.

### Features

- Ultra low quiescent current ( IQ = 45uA)
- Wide supply voltage: 3.7 - 20.0V
- Peak segment drive current 30mA
- Segment switching time: 650mS
- Simple SPI 3 wire interface

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### Block Diagram



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## Functional Description

Figure 2 shows the input data format. At rest CLOCK, DATA IN and LATCH ENABLE are all low. The transition of LATCH ENABLE from logic "0" to logic "1" signals the start of transmission.

Serial Data present at DATA IN is transferred to the shift register on the logic "1" to logic "0" transition of the CLOCK input pulse. On the following CLOCK pulses, the register shifts data towards DATA OUT. The serial data must be stable before the falling edge of the CLOCK and must be held stable after the falling edge. See timings.

The transition of LATCH ENABLE from logic "1" to logic "0" signals the end of transmission and if bit 8 of the shift register = "0" data is transferred to the segment latches. If bit 8 of the shift register = "1" the transmission contains a Command, see below for list Commands.

A RESET input is available. This line should be driven by an open collector driver and is active low. Asserting the reset disables the common anode and segment drivers and resets all Command parameters to the default state. The PCB does not require a RESET signal for proper operation. If this feature is not used leave the RESET input unconnected.

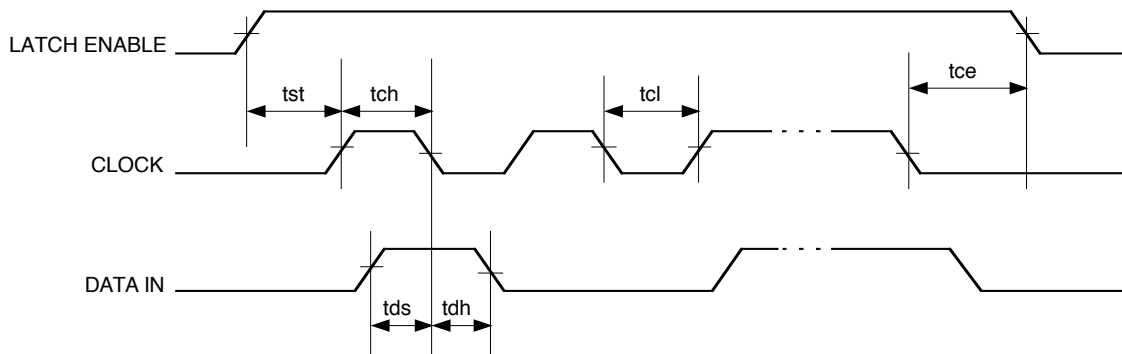


Figure 2. Input Data timing

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## Application notes:

The CXL-SD150S display driver PCB has a wide input supply range with an on board voltage regulator. Internally the PCB runs at +3.3V with +5.0V tolerant inputs on CLOCK, DATA IN and LATCH ENABLE making interfacing to existing designs simple.

The unique properties of the Ntera Nanochromics 7 segment display allow extremely low power displays with exceptional viewing angle and contrast ratio to be constructed. The displays are essentially bi-stable. To the driver the segments appear to be a large capacitor. The segments have a capacitance of approximately 10,000 $\mu$ F per square cm.

Charged segments need to be periodically refreshed to replenish the small leakage charge. The driver PCB does this automatically.

The driver PCB is designed for easy cascading using 20 way ribbon cable. If a more than 10 digits are to be cascaded it would probably be advantageous to feed power into the ribbon cable from both ends.

The CXL-SD150S PCB is well suited to battery operation and a number of Commands are available allowing the segment switching current to be programmed and the refresh cycles to be staggered between digits. These Commands are used to limit the peak battery load.

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# Commands

This page is under construction.

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## Interface connector

### P1 pinout

Pin Name	Pin no.	Description
GND	1,2,3,4	Power Ground
NC	5	Do not connected
RESET	6	Reset, active low
NC	7	Do not connect
LATCH ENABLE	8	Latch Enable
DATA IN	9	Data In
CLOCK	10	Clock
NC	11 - 16	Do not connect
VIN	17,18,19,20	Power +

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## ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

Supply voltage (VIN) 25V  
Logic Inputs (CLOCK, DATA IN LATCH ENABLE) 6.5V

### DC Electrical Characteristics

TA = +25°C, VIN = 5.0V

Parameter	Sym	Conditions	Min	Typ	Max	Units
Supply Voltage	VIN		3.7	5.0	20	V
Quiescent Current	IQ	Display Static			50	μA
Segment On Current	ION	Single segment switching On		25		mA
Segment Off Current	IOFF	Single segment switching Off		25		mA
Peak Current	IPK	All segments switching		160		mA
Input Low Voltage	VIL	Clock, Data In, Latch Enable	0		0.5	V
Input High Voltage	VIH	Clock, Data In, Latch Enable	2.65		5.0	V

### AC Electrical Characteristics

VIN = 5.0V

Symbol	Parameter	Min	Typ	Max	Units
tst	Latch Enable high to Clock high	20		1000	μs
tch	Clock high	0.5	5		μs
tcl	Clock low	0.5	5		μs
tds	Data In setup time	100			ns
tdh	Data In hold time	100			ns
tce	Clock low to Latch Enable low	10			μs

# Dimensions

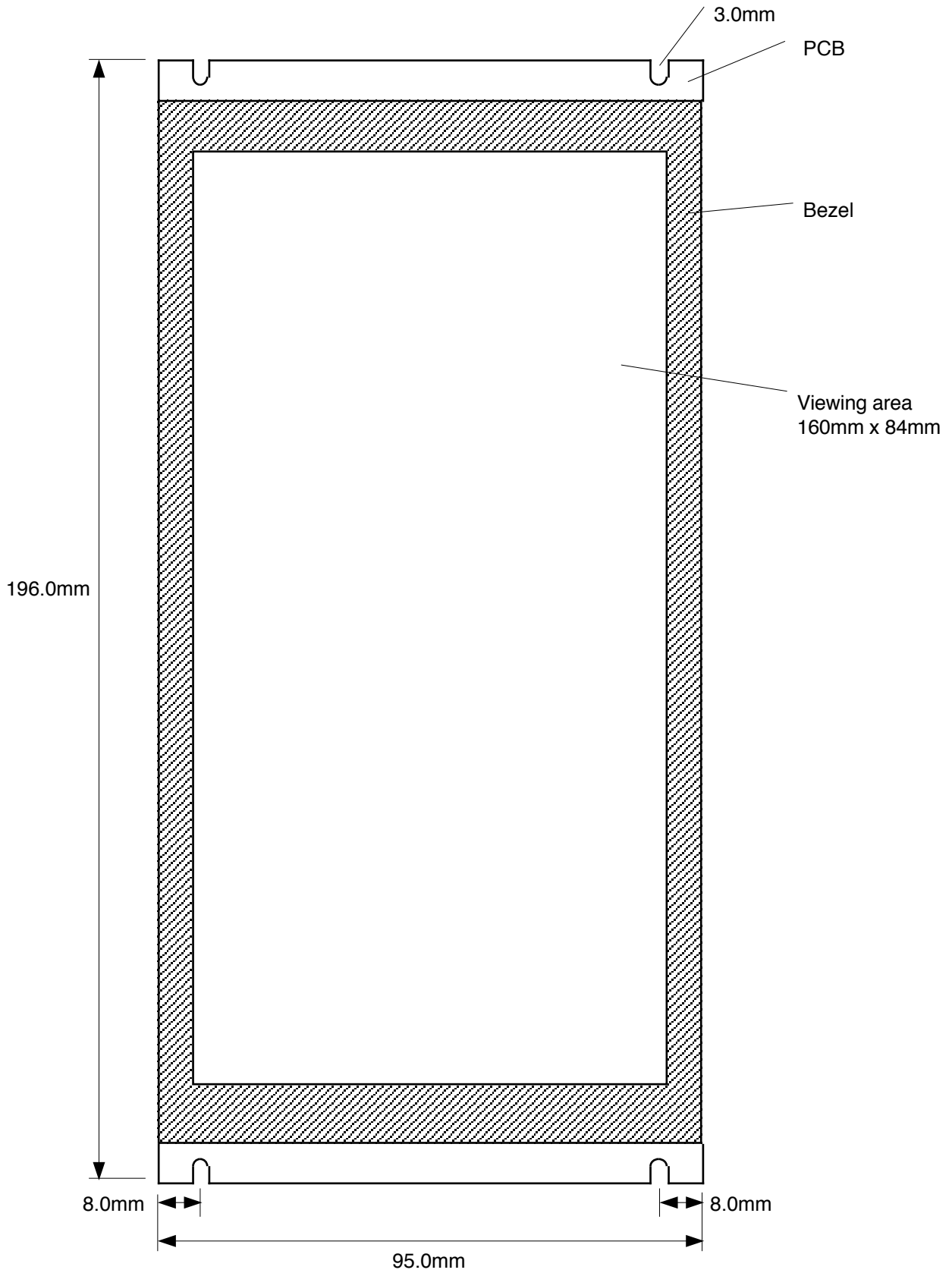


Figure 3. Front View of PCB with display glass and bezel

Dimensions cont.

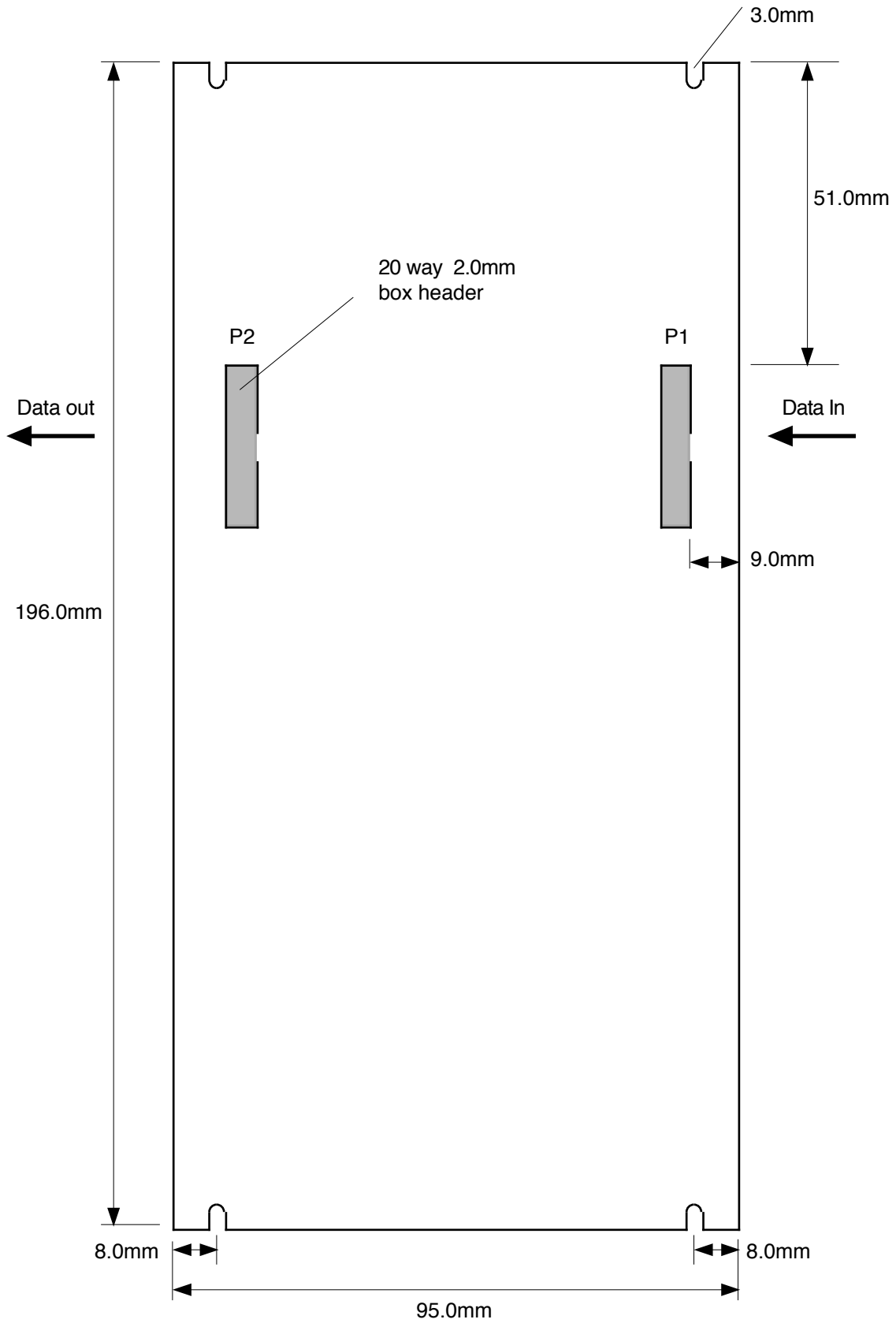


Figure 4. Rear view of PCB showing connector position